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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/757,186
Filing Date: January 14, 2004
Appellant(s): DEWITT ET AL.

Gerald H. Glanzman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/29/2008 appealing from the Office action mailed 11/29/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

((4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct. **Note that the appellant does NOT appeal the 35 USC 101 Rejection.**

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,691,920	LEVINE ET AL	11-1997

Applicants' acknowledged prior art

Morris Mano, "Computer System Architecture", 1982, Prentice-Hall, Inc., 2nd Ed., pp 434-443.

Definition of "Interrupt" by Wikipedia.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-7 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "interrupt unit control mechanism," "interrupt unit," and "performance monitoring unit" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 2172.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function simultaneously, are directly functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.

If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state on the record that this is the case.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the language "responsive ... control register" (lines 11-12) lack clear support from the specification. See also the 35 USC 112, 2nd paragraph above.

Claim Rejections - 35 USC § 101

Claims 16 and 23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

With regard to claims 16 and 23, as disclosed in the specification, the computer readable medium can be a "digital and analog communication links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions." It is clear that "radio frequency and light wave transmissions" may transmit but simply cannot store and record any instruction; and are not a tangible media.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-12, and 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Levine et al. (U.S. Patent No. 5,691,920).

Referring to claim 1: Levine discloses a performance-monitoring unit (Abstract) and one or more hardware counters (column 10, lines 58-59) located within the performance-monitoring unit (figure 4, structures 50 and 51). Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-56); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Furthermore, Levine disclosed two separate counters for selected events (figure 6A, column 8, lines 57-60). It is also clear that in Levine, at least bits 5 and 16 in a register field of a particular MMCR associated with a particular counter PMC indicate "an interrupt of a selected type" or specifically, the performance monitoring interrupt type. In other words, the type of interrupt indicated and associated with MMCR shown below is the performance monitoring interrupt type.

BITS 0-4 COUNTING ENABLES	BIT 5 INTERRUPT ENABLE	BITS 6-15	BIT 16 PMC1 INTERRUPT CONTROL	BIT 17 PMCn, n>1 COUNT CONTROL	BIT 18 PMCn, n>1 COUNT CONTROL	BITS 19-25 PMC1 EVENT SELECTION	BITS 26-31 PMC2 EVENT SELECTION

MONITOR MODE CONTROL REGISTER 0
(MMCR0)

FIGURE 6A

Further, it is also clear the performance monitoring interrupt is presented to the interrupt resolution logic or interrupt handler 57, which uses a plurality of interrupt handling routines to serve the interrupts depending from the types of interrupts. In other words, depending on a particular type of interrupt, the interrupt handler 57 will select a particular interrupt handling routine among the plurality of interrupt handling routines employed by the interrupt handler 57. It is clear that the interrupt handler 57 MUST be able to determine which type of interrupt presented to it before it selects the corresponding interrupt handling routine accordingly. In the instant case, the interrupt handler 57 must be able to determine that the presented interrupt is the performance monitoring interrupt before it selects a routine designed for performance monitoring. Thus, it is clear that the interrupt resolution logic or interrupt handler 57 is readable as the "interrupt unit."

Referring to claims 2-3: Since the nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine; thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 4: Levine discloses monitoring instruction execution and storage control (column 1, lines 65), which are the claimed multiple types of events.

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claims 8-10: It is clear that the states of the performance monitor interrupt include at least the state wherein an interrupt signal is generated, and a state wherein the interrupt is serviced or processed. As discussed above, during processing the performance monitor interrupt, multiple events are counted by hardware counters located inside the performance monitor unit 50. The counters count the events during the interrupt service routine, which is a "state" of the performance monitor interrupt.

Referring to claim 11: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses

are a selected interrupt handling routine, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; furthermore, Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Since Levine discloses that it is preferred to examine all stages, Levine discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt.

Referring to claim 17: The nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine.

Referring to claim 18: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses are a selected interrupt handling routine, Levine's performance-monitoring unit's one or

more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6, 8-14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Levine.

Referring to claim 1: The admitted prior art discloses a performance-monitoring unit (Specification, page 3, last paragraph, line 6) and one or more hardware counters (Specification, page 3, last paragraph, lines 1-2) located within the performance-monitoring unit. The admitted prior art does not disclose that the one or more hardware counters count the occurrence of events during an interrupt of a selected type.

Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-39); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck.

Referring to claim 2: Since an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine (Specification, page 4, 2nd paragraph, lines 3-11); thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 3: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 4: The admitted prior art discloses monitoring multiple types of events (Specification, page 3, last paragraph, lines 3-4, page 4, 1st paragraph, lines 5-7).

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claims 8-9: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt. However, in Levine, it is clear that the states of the performance monitor interrupt include at least the state wherein an interrupt signal is generated, and a state wherein the interrupt is serviced or processed. As discussed above, during servicing or processing the performance monitor interrupt, multiple events are counted by hardware counters located inside the performance monitor unit 50. The counters count the occurrence of events during the interrupt service routine, which is a "state" of the performance monitor interrupt.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 10: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 11: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Levine's examination on all stages are the claimed counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine teaches one on how to locate the performance bottleneck by tracing the processing through all stages.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 17: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 18: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Claims 7, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Levine in view of previously cited "Computer System Architecture" by Morris Mano or as being unpatentable over the admitted prior art in view of Levine and Mano.

Referring to claims 7, 15, and 22: The disclosures of the admitted prior art and Levine are stated above. As stated above, Levine discloses monitoring the particular interrupt according to the instructions address, and Levine discloses two separate counters for event selections (figure 6A, column 8, lines 57-60); thus, Levine discloses the hardware counters counting events separately. But neither explicitly discloses a second interrupt interrupts a first interrupt.

Mano discloses managing interrupt according to its priority (pages 434-435). Mano discloses that a higher priority interrupt can interrupt an in-process lower priority interrupt (page 435, 2nd paragraph). Mano teaches one to manage the limited system resources by prioritizing interrupt. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Mano's teaching onto the admitted prior art and Levine because Mano teaches one to manage the limited system resources by prioritizing interrupt.

(10) Response to Argument

35 USC 112, 2nd Paragraph Rejection:

Appellants have argued that "claims 1-7 are definite and the inter- relationship of the components are set forth in the last element of claim 1, which recites 'one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events that occur during processing of the interrupt responsive to a determination by the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt

unit control register of the selected type.' Thus, the hardware counters are located within the performance monitoring unit and the hardware counters count the occurrence events in response to the interrupt unit determining that the interrupt is of an interrupt type that has been selected to be monitored. The interrupt unit determines this by checking the interrupt unit control registers, which indicate the interrupt type that is to be monitored. The specification fully supports this interpretation on page 21, line 17 - page 22, line 2, and page 25, line 28 - page 27, line 6; Figure 5."

In response to Appellants' argument, it is noted that Appellants' argument does not relate to the rejection at all. Specifically, the "hardware counters" were NOT at all mention in the rejection. As clearly set forth above in the 35 USC 112, 2nd Paragraph, claims 1-7 are directed to an apparatus. However, the essential structural cooperative relationships between the so-called "interrupt unit control mechanism," "interrupt unit," and "performance monitoring unit" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 2172.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function simultaneously, are directly

functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.

35 USC 112, 1st Paragraph Rejection:

With regard to the rejection under 35 USC 112, 1ST Paragraph (New Matter), Appellants have argued that "Appellants respectfully disagree with the Examiner's position. Appellants submit that the specification, on page 21, line 17 - page 22, line 2, fully supports the recited feature of "responsive to a determination by the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." The specification, on page 21, line 26-28, states "IUCR such as IUCR1 308 includes a type field that indicates which interrupt type is to generate a performance monitoring counter signal." Thus, the specification clearly supports that the interrupt unit control register indicates the interrupt type selected to be monitored. Further, on page 21, line 28 - page 22, line 2, the specification states "The type field in the IUCR is later examined by interrupt unit 304 to see if it is an interrupt type of interest, i.e., whether events are to be counted during execution of the interrupt." Thus, the specification clearly supports that the interrupt unit determines that the interrupt is of the interrupt type to be monitored as indicated by the interrupt unit control register, as the specification states that interrupt unit 304 examines the interrupt unit control register to see if the interrupt is an interrupt type of interest. Further Figure 5 and the text describing Figure 5 on page 25, line 28 - page 27, line 6, also describe this process in detail. Specifically, the specification states, "When an interrupt occurs during

code execution (step 512), the interrupt unit examines the IUCR type field (step 514). A determination is made as to whether the interrupt is the same type as the IUCR type, which is an interrupt type of interest (step 516)." Thus, the specification clearly supports the claimed feature of "responsive to a determination by the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." Thus, Appellants submit that the specification clearly supports the feature of "responsive to a determination by the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." Further, claims 2-7 were rejected on the basis of depending from claim 1."

In response to Appellants' argument, at the outset, claim 1 is reproduced below for ease of reference and convenience.

1. A data processing system for qualifying events when an interrupt occurs, comprising:

an interrupt unit control register for indicating an interrupt type selected to be monitored;

an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register;

a performance monitoring unit; and

one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register.

The phrase, "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" is taken out of context. While the Examiner agrees with Appellants that "the specification clearly supports that the interrupt unit determines that the interrupt is of the interrupt type to be monitored as indicated by the interrupt unit control register," The Examiner disagrees with Appellants that the specification supports the language, "wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." In other words, the phrase, "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" when understood in context of the above cited limitation, does not have adequate support from the specification.

35 USC 101 Rejection:

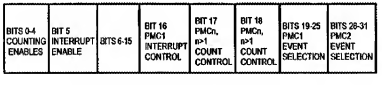
Appellants do not appeal the 35 USC 101 Rejection.

35 USC 102 Rejection:

Appellants have argued that "[i]nitially, Levine does not disclose or in any way suggest, 'an interrupt unit control register for indicating an interrupt type selected to be monitored' as presently recited in claim 1. Levine does not describe interrupt types and does not disclose a register that indicates an interrupt type selected to be monitored.

Bits 5 and 16 illustrated in Figure 6A of Levine reproduced by the Examiner are not interrupt types selected to be monitored, but, at best, may relate to states of an interrupt."

Contrary to Appellants' argument, it is clear from Levine that the "MMCR0 [Monitor Mode Control Register 0] is partitioned into a number of bit fields whose settings **select events to be counted, enable performance monitor interrupts**, specify the conditions under which counting is enabled, and set a threshold value (X) " (emphasis added). See Levine, column 12, lines 4-11. The MMCR0 (Monitor Mode Control Register 0), as shown in Fig. 6a, is included in the Performance Monitor 50 and is used to control the operation of two PCM (Performance Monitor Counter) counters, e.g., PCM1 and PCM2. See Levine, column 9, lines 55-58, and column 12, lines 1-3. Fig. 6a is reproduced below for ease of reference and convenience.



MONITOR MODE CONTROL REGISTER 0
(MMCR0)

FIGURE 6A

As shown above in Fig. 6a, **it is clear that bit 5 represents Performance Monitor Interrupt, which is a particular type of interrupt**; and **setting of bit 5 will enable the Performance Monitor Interrupt**. See "BIT 5 Interrupt Enable" field in Fig. 6a above. Also, as shown in Fig. 6a above, bit 16 is "PCM1 Interrupt Control" for controlling interrupt signals triggered by PMC (Performance Monitor Counter]). See

column 12, lines 59-60. The MMCR0 (Monitor Mode Control Register 0) is also used to set a threshold value (X). See column 12, lines 4-11. The Performance Monitor Counter, e.g., PCM1, increments every time the threshold value is exceeded. See column 12, lines 25-26. Whenever a predetermined value for the counter is reached, the Performance Monitor Interrupt is signaled. See column 12, lines 28-34. The Performance Monitor 50 then uses the Performance Monitoring Interrupt to interrupt all activities of the processors, and start performance monitoring. See column 10, lines 56-57, and column 11, lines 15-30.

As shown in Fig. 4 below, the Performance Monitor Interrupt (IRQ) is generated whenever the bit 5 of the MMCR0 (Monitor Mode Control Register 0) is set. The MMCR0 and the PMC (Performance Monitor Counter) are included in the Performance Monitor 50. When the predetermined value of the Performance Monitor Counter PCM1 (for example) is reached, bit 5 indicating a specific type of interrupt called "Performance Monitoring Interrupt" is set, and in response to the setting of bit 5, the Performance Monitor generates the Performance Monitor Interrupt.

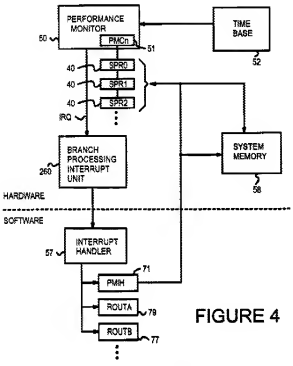


FIGURE 4

In other words, the Monitor Mode Control Register (interrupt unit control as claimed) is used for indicating the Performance Monitor Interrupt selected to be monitored by the Performance Monitor 50 so that whenever bit 5 of the register is set, the Performance Monitor 50 generates the Performance Monitor Interrupt.

Appellants have also argued that "Levine does not disclose "an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as recited in claim 1. In rejecting the claims, the Examiner construes the interrupt handler 57 in Levine as corresponding to the interrupt unit recited in claim 1. In particular, the Examiner points out that interrupt handler 57 in Levine selects one of interrupt handling routines 71, 77 and 79 illustrated in Figure 4, and concludes "[i]t is clear that the interrupt handler 57 MUST be able to determine

which type of interrupt presented to it before it selects the corresponding interrupt handling routine accordingly." Appellants respectfully disagree. Appellants respectfully submit that Levine nowhere discloses or suggests that interrupt handler 57 selects any of interrupt handling routines 71, 77 and 79 based on interrupt type, and Levine certainly does not disclose that interrupt handler 57 selects a particular interrupt handling routine based on an interrupt type selected to be monitored. Neither the Monitor Mode Control Register illustrated in Figure 6A referred to by the Examiner nor the discussion of the interrupt handling routines in column 9, lines 46-62 in Levine suggests that interrupt handler 57 selects a particular interrupt routine based on interrupt type. Rather, Levine merely teaches, in column 9, lines 46-62, that interrupt resolution logic passes the interrupt to one of various interrupt handler routines. However, passing an interrupt to one of multiple interrupt handling routines has nothing to do with determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register. Even assuming arguendo that the interrupt handler selects a specific interrupt handler routine based on a type of interrupt, selecting an appropriate interrupt handler routing is not the same as, and has nothing to do with "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." Levine does not disclose that interrupt handler 57 functions to be "responsive to an interrupt occurring during code execution for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as recited in claim 1" (emphasis in the original).

Contrary to Appellants' argument, as discussed above, the Performance Monitor Interrupt (IRQ) is generated whenever the bit 5 of the MMCR0 (Monitor Mode Control Register 0) is set. The MMCR0 and the PMC (Performance Monitor Counter) are included in the Performance Monitor 50. When the predetermined value of the Performance Monitor Counter PCM1 (for example) is reached, bit 5 for indicating a specific type of interrupt called "Performance Monitoring Interrupt" is set, and in response to the setting of bit 5, the Performance Monitor generates the Performance Monitor Interrupt. **In other words, the Monitor Mode Control Register (interrupt unit control as claimed) is used for indicating the Performance Monitor Interrupt selected to be monitored by the Performance Monitor 50 so that whenever bit 5 of the register is set, the Performance Monitor 50 generates the Performance Monitor Interrupt.**

Further, as described by Levine in the specification, column 9, lines 46-52, the Performance Monitor Interrupt is then presented to the interrupt resolution unit or interrupt handler 57, which employs various interrupt handling routines 71, 77, and 79. Since the Performance Monitor Interrupt is a specific type of interrupt. Therefore, it is clear that a specific routine for performance monitoring must be selected to service the specific Performance Monitoring Interrupt. As a matter of fact, Levine clearly discloses that the performance monitoring routine is "**selected**." See column 10, lines 43-45. In response to Appellants' argument that "[e]ven assuming arguendo that the interrupt handler selects a specific interrupt handler routine based on a type of interrupt, selecting an appropriate interrupt handler routing is not the same as, and has nothing to

do with "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register," it is noted that the Examiner never equates selecting a specific interrupt handler routine based on a type of the interrupt with "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as alleged by Appellants. Appellants are directed to discussion above regarding limitation: "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

In addition, Appellants also have argued that "Levine also does not disclose or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." Although Levine may disclose counters in performance monitor 50 illustrated in Figure 4 of Levine, the counters are described as being for counting processor/storage related events" (see col. 8, lines 33-41 of Levine). Levine does not disclose that the counters count events that occur during processing of an interrupt 'responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register' as required in claim 1. Levine does not disclose interrupt types and does not determine if an interrupt that occurs during code execution is of an interrupt type selected to be monitored."

In response to Appellants' argument, at the outset, it is noted that the phrase, "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" when understood in context of the above cited limitation, does not have adequate support from the specification. See the 35 USC 112, 1st Paragraph Rejection above.

In any event, contrary to Applicants' argument, Levine, as a matter of fact, discloses one or more hardware counter located within the performance monitoring unit. As clearly shown in Fig. 4, which is reproduced below;

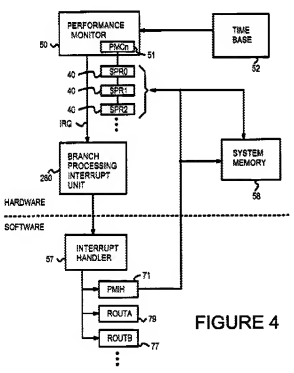


FIGURE 4

one or more hardware counters PMCn 51 are located within the performance monitor 50. See column 8, lines 37-56. As also disclosed by Levine, the performance monitor 50 3is intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the

performance monitor 50 includes Performance Monitor Counter 51 for counting processor/storage **related events**. See at least column 8, lines 33-41, column 9, line 63 to column 10, line 32. Further, as discussed above, the Performance Monitor Interrupt (IRQ) is generated whenever the bit 5 of the MMCR0 (Monitor Mode Control Register 0) is set. The MMCR0 and the PMC (Performance Monitor Counter) are included in the Performance Monitor 50. When the predetermined value of the Performance Monitor Counter PCM1 (for example) is reached, bit 5 for indicating a specific type of interrupt called "Performance Monitoring Interrupt" is set, and in response to the setting of bit 5, the Performance Monitor generates the Performance Monitor Interrupt. During "processing" of the Performance Monitoring Interrupt, at least one counter PCM (Performance Monitor Counter) is used to capture data for performance analysis; and each counter has a pre-assigned event to be monitored. See column 11, lines 66-67, and column 14, lines 12-13. Specifically, the performance monitoring is achieved by using the PCMn (Performance Monitor Counter) and configuring them with the MMCRn (Monitor Mode Control Register) to count events that effect performance such as stalls. See column 15, lines 10-21, lines 53-62, and column 23, lines 14-39. Thus, it is clear from discussion above that the counters count events that occur during processing of an interrupt "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as required in claim 1.

With regard to claim 8, Appellants have argued that "Levine does not disclose an invoked interrupt that includes a plurality of states, and also does not disclose counting at least one event for a selected state of the plurality of states during processing of the invoked interrupt. Rather, in column 9, lines 55-62, Levine teaches that when an interrupt is generated (signaled), the state of various execution units are saved in a saved state register (SSR). Further, when the interrupt is actually serviced, the content of the SSR provides information concerning instructions at the time of signaling the interrupt. In contradistinction, claim 8 recites, "counting at least one event for a selected state of the plurality of states during processing of the invoked interrupt." Thus, Levine teaches providing state information of the system at the time the interrupt was generated; whereas claim 8 recites, 'counting at least one event for a selected state of the plurality of states during processing of the invoked interrupt.' Thus, Levine fails to teach the feature of 'counting at least one event for a selected state of the plurality of states during processing of the invoked interrupt.' Furthermore, nothing in Levine teaches, 'wherein the invoked interrupt includes a plurality of states.' Rather, as taught by Levine, when an interrupt is generated, state information of various execution units is saved to SSRs. Nothing in Levine teaches that the generated interrupt 'includes a plurality of states.' Therefore, Levine fails to teach the feature of 'receiving a signal at a microprocessor of the data processing system for invoking an interrupt, wherein the invoked interrupt includes a plurality of states.'"

Contrary to Appellants' argument, as discussed above with regard to claim 1, the Performance Monitor Interrupt (IRQ) is generated whenever the bit 5 of the MMCR0

(Monitor Mode Control Register 0) is set. Bit 5 (see Fig. 6a above) indicates a specific type of interrupt, namely the "Performance Monitor Interrupt." When the predetermined value of the Performance Monitor Counter PCM1 (for example) is reached, bit 5 for indicating a specific type of interrupt called "Performance Monitoring Interrupt" is set, and in response to the setting of bit 5, the Performance Monitor generates the Performance Monitor Interrupt. The Performance Monitor Interrupt ("interrupt" as claimed) is represented by bit 5, wherein transition or flip of bit 5 changes the state of bit 5. For example, as discussed above, setting of bit 5 (change the state of bit 5 from one state to another) enables the Performance Monitor Interrupt. Thus, the plurality of states includes a state wherein the interrupt from a processor is received, and the bit 5 has not been set to indicate a particular interrupt ("interrupt on"), setting the bit 5 to enable the Performance Monitor Interrupt ("interrupt taken"), and clearing (transition) bit 5 ("interrupt acknowledged"). Further, as discussed above, during "processing" of the Performance Monitoring Interrupt, wherein the state of bit 5 has not been set, at least one counter PCM (Performance Monitor Counter) is used to capture data for performance analysis; and each counter has a pre-assigned event to be monitored. See column 11, lines 66-67, and column 14, lines 12-13. Specifically, the performance monitoring is achieved by using the PCMn (Performance Monitor Counter) and configuring them with the MMCRn (Monitor Mode Control Register) to count events that effect performance such as stalls. See column 15, lines 10-21, lines 53-62, and column 23, lines 14-39.

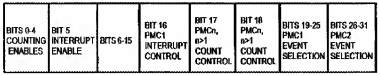
The 103 Rejection:

With regard to claims 1-6, 8-14, and 16-21, Applicants argued that: "[i]n the present case, neither the admitted prior art nor Levine nor their combination discloses or suggests 'an interrupt unit control register for indicating an interrupt type selected to be monitored', 'an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register', or 'one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register' as recited in claim 1. Levine does not disclose the subject matter of claim 1 for reasons discussed in detail above in Section C. The admitted prior art is cited as only disclosing a performance monitoring unit having hardware counters. The admitted prior art does not teach the features of 'an interrupt unit control register for indicating an interrupt type selected to be monitored', 'an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register', or 'one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register.' Thus the

admitted prior art fails to teach or suggest these features. Accordingly, neither the admitted prior art, Levine, nor the combination of the admitted prior art in view of Levine teaches all of the features of the claimed invention as recited in claim 1. Thus, the Examiner has not established a prima facie case of obviousness in rejecting claim 1."

In response to Appellants' argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). As discussed above, the acknowledged prior art discloses "one or more hardware counter located within the performance monitoring unit."

As discussed above with regard to the rejection of claim 1, it is clear from Levine that the "MMCR0 [Monitor Mode Control Register 0] is partitioned into a number of bit fields whose settings **select events to be counted, enable performance monitor interrupts**, specify the conditions under which counting is enabled, and set a threshold value (X) " (emphasis added). See Levine, column 12, lines 4-11. The MMCR0 (Monitor Mode Control Register 0), as shown in Fig. 6a, is included in the Performance Monitor 50 and is used to control the operation of two PCM (Performance Monitor Counter) counters, e.g., PCM1 and PCM2. See Levine, column 9, lines 55-58, and column 12, lines 1-3. Fig. 6a is reproduced below for ease of reference and convenience.



MONITOR MODE CONTROL REGISTER 0
(MMCR0)

FIGURE 6A

As shown above in Fig. 6a, **it is clear that bit 5 represents Performance Monitor Interrupt, which is a particular type of interrupt**; and **setting of bit 5 will enable the Performance Monitor Interrupt**. See "BIT 5 Interrupt Enable" field in Fig. 6a above. Also, as shown in Fig. 6a above, bit 16 is "PCM1 Interrupt Control" for controlling interrupt signals triggered by PMC (Performance Monitor Counter]). See column 12, lines 59-60. The MMCR0 (Monitor Mode Control Register 0) is also used to set a threshold value (X). See column 12, lines 4-11. The Performance Monitor Counter, e.g., PCM1, increments every time the threshold value is exceeded. See column 12, lines 25-26. Whenever a predetermined value for the counter is reached, the Performance Monitor Interrupt is signaled. See column 12, lines 28-34. The Performance Monitor 50 then uses the Performance Monitoring Interrupt to interrupt all activities of the processors, and start performance monitoring. See column 10, lines 56-57, and column 11, lines 15-30.

As shown in Fig. 4 below, the Performance Monitor Interrupt (IRQ) is generated whenever the bit 5 of the MMCR0 (Monitor Mode Control Register 0) is set. The MMCR0 and the PMC (Performance Monitor Counter) are included in the Performance Monitor 50. When the predetermined value of the Performance Monitor Counter PCM1

(for example) is reached, bit 5 indicating a specific type of interrupt called "Performance Monitoring Interrupt" is set, and in response to the setting of bit 5, the Performance Monitor generates the Performance Monitor Interrupt.

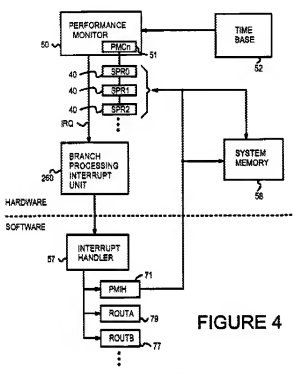


FIGURE 4

In other words, the Monitor Mode Control Register (interrupt unit control as claimed) is used for indicating the Performance Monitor Interrupt selected to be monitored by the Performance Monitor 50 so that whenever bit 5 of the register is set, the Performance Monitor 50 generates the Performance Monitor Interrupt.

As noted above, Levine discloses that the Performance Monitor Interrupt (IRQ) is generated whenever the bit 5 of the MMCR0 (Monitor Mode Control Register 0) is set. The MMCR0 and the PMC (Performance Monitor Counter) are included in the Performance Monitor 50. When the predetermined value of the Performance Monitor Counter PCM1 (for example) is reached, bit 5 for indicating a specific type of interrupt

called "Performance Monitoring Interrupt" is set, and in response to the setting of bit 5, the Performance Monitor generates the Performance Monitor Interrupt. In other words, the Monitor Mode Control Register (interrupt unit control as claimed) is used for indicating the Performance Monitor Interrupt selected to be monitored by the Performance Monitor 50 so that whenever bit 5 of the register is set, the Performance Monitor 50 generates the Performance Monitor Interrupt.

Further, as described by Levine in the specification, column 9, lines 46-52, the Performance Monitor Interrupt is then presented to the interrupt resolution unit or interrupt handler 57, which employs various interrupt handling routines 71, 77, and 79. Since the Performance Monitor Interrupt is a specific type of interrupt. Therefore, it is clear that a specific routine for performance monitoring must be selected to service the specific Performance Monitoring Interrupt. As a matter of fact, Levine clearly discloses that the performance monitoring routine is "**selected.**" See column 10, lines 43-45. In response to Appellants' argument that "[e]ven assuming arguendo that the interrupt handler selects a specific interrupt handler routine based on a type of interrupt, selecting an appropriate interrupt handler routing is not the same as, and has nothing to do with "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register," it is noted that the Examiner never equates selecting a specific interrupt handler routine based on a type of the interrupt with "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as alleged by Appellants. Appellants are directed to discussion above regarding limitation: "determining whether

the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." Further, Levine, as a matter of fact, discloses one or more hardware counter located within the performance monitoring unit. See column 8, lines 37-56. As also disclosed by Levine, the performance monitor 50 is intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the performance monitor 50 includes Performance Monitor Counter 51 for counting processor/storage **related events**. See at least column 8, lines 33-41, column 9, line 63 to column 10, line 32. Further, as discussed above, the Performance Monitor Interrupt (IRQ) is generated whenever the bit 5 of the MMCR0 (Monitor Mode Control Register 0) is set. The MMCR0 and the PMC (Performance Monitor Counter) are included in the Performance Monitor 50. When the predetermined value of the Performance Monitor Counter PCM1 (for example) is reached, bit 5 for indicating a specific type of interrupt called "Performance Monitoring Interrupt" is set, and in response to the setting of bit 5, the Performance Monitor generates the Performance Monitor Interrupt. During "processing" of the Performance Monitoring Interrupt, at least one counter PCM (Performance Monitor Counter) is used to capture data for performance analysis; and each counter has a pre-assigned event to be monitored. See column 11, lines 66-67, and column 14, lines 12-13. Specifically, the performance monitoring is achieved by using the PCMn (Performance Monitor Counter) and configuring them with the MMCRn (Monitor Mode Control Register) to count events that effect performance such as stalls. See column 15, lines 10-21, lines 53-62, and column 23, lines 14-39. Thus, it is clear from discussion

above that the counters count events that occur during processing of an interrupt "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as required in claim 1.

Further, as clearly stated in the 103 Rejection, the benefits and advantages are readily realized by employing the performance monitor taught by Levine. As set forth in MPEP Section 2144, "the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983)." In the instant case, the advantage or expected beneficial result, which would have been produced by the combination, is a significant improvement in system performance, obtained by indicating and resolving performance bottlenecks or stalls.

With regard to claims 7, 15, and 22, Applicants argued that "Claims 7, 15, and 22 depend from and further restrict one of independent claims 1, 8, and 16. Mano does not cure the deficiencies in Levine or in the admitted prior art in view of Levine as discussed above. Mano discloses managing interrupts according to a priority for the interrupt. Mano is silent in regards to the features of 'an interrupt unit control register for indicating an interrupt type selected to be monitored', 'an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control

register', or 'one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register.' Thus Mano fails to teach or suggest the feature of 'an interrupt unit control register for indicating an interrupt type selected to be monitored', 'an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register', or 'one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register," as recited in claim 1."

In response to Appellants' argument, Applicants cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In any event, Appellants are directed to the disclosure of Levine discussed above in the rejection of claim 1. As already noted in the Final Rejection, an interrupt (second interrupt, for example), by definition, interrupts another interrupt process (first interrupt, for example). See definition of Interrupt by Wikipedia, previously cited. As a secondary reference, Mano discloses managing interrupt according to its priority (pages 434-435).

Mano discloses that a higher priority interrupt can interrupt an in-process lower priority interrupt (page 435, 2nd paragraph). Mano teaches one to manage the limited system resources by prioritizing interrupt. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Mano's teaching onto the admitted prior art and Levine because Mano teaches one to manage the limited system resources by prioritizing interrupt.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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